

U.S.S.N. 10,797,945

Remarks

Thorough examination by the Examiner is noted and appreciated.

The claims have been amended to overcome Examiner objections and rejections and to clarify Applicants invention and new claims have been added.

Support for the new claims is found in the original claims, The Specification and The Figures.

No new matter has been added.

For example support for the amendments and new claims is found in Figure 1E, and the Specification at:

Paragraph 0021:

"Preferably, the aspect ratio, defined herein as the contact opening depth/ contact opening width at the bottom portion of the contact opening, is preferably less than about 3.3 with the contact opening width at the bottom portion of the contact hole being less than about 70 nm. Thus the thickness of the first ILD layer following planarization including optional deposition of one or more of a hardmask layers and overlying inorganic or organic anti-reflectance (ARC) coatings, is preferably less than about 2350 Angstroms to form with the preferred contact opening aspect ratio. More preferably, the aspect ratio for the contact hole formed in the first ILD layer is less than

U.S.S.N. 10,797,945

about 4.5 with a contact opening width (bottom portion) less than about 50 nm."

Paragraph 0026:

"Referring to Figure 1F, a similar process as outlined for forming the first set of contact interconnects 30A, 30B, 30C, 30D, and 30E is then carried out to form a second set of contact interconnects e.g., 32A, 32B, and 32C extending through the thickness of the second ILD layer 22B to make contact (e.g., including overlying and at least partially encompassing) portions of the first set of contact interconnects. The second set of contact interconnects is formed according to the same preferred embodiments and aspect ratios as the first set of contact interconnects the first ILD layer 22A. The second set of contact interconnects may have the same or different preferred aspect ratio as the second set of contact interconnects, for example having a smaller aspect ratio to ensure adequate interconnect overlap. In addition, longer (horizontal to the substrate) contact interconnects e.g., 32A may be formed to conductively connect one or more of the first set of contact openings e.g., 30A and 30B. Preferably, the length of the longer contact interconnects, e.g., 32A is between about 0.15 microns and about 500 microns.

Claim Objections

The claims including 18, 26, 30 and 34 have been amended to overcome Examiners objections.

Claim Rejections under 35 USC 112

Claim 31 has been cancelled to overcome Examiners rejection.

U.S.S.N. 10,797,945

Claim Rejections under 35 USC 103

1. Claims 18-25 and 27-31 stand rejected under 35 USC Section 103(a) as being unpatentable over Karasawa et al. (US 6,720,628) in view of Zhou et al. (US 6,358,842) and Chen et al. (6,784,096).

Karasawa discloses an interconnect structure where a wiring layer (32a, 40, 42) is provided between a lower contact structure (80, 82) and an upper interconnect structure (84) in an upper contact layer (92) (see Figure 13; col 10, lines 46-63; col 11, lines 41-49; col 12, lines (col 12, lines 34-44). Karasawa fails to disclose several aspects of Applicants disclosed and claimed invention including:

"A contact interconnect structure comprising:

a semiconductor substrate comprising CMOS devices including active contact regions;

a first contact layer overlying the active contact regions comprising a first plurality of metal filled openings extending through the first contact layer thickness to the active contact regions;

a second contact layer overlying the first contact layer

U.S.S.N. 10,797,945

comprising a second plurality of metal filled openings, each of said second plurality of metal filled openings **extending through the second contact layer thickness to a respective one or more of the first plurality of metal filled openings;**

wherein, each of the first second plurality of metal filled openings **form a continuously connected contact interconnect structure** having an aspect ratio of less than about 4.5 with respect to a respective contact layer."

On the other hand, Zhou et al. discloses a single or dual damascene interconnect structure (see Abstract; Figures). Zhou et al. nowhere discloses a contact interconnect structure extending to active contact regions.

Also in contrast to Karasawa, Chen et al. disclose a method of **forming a barrier layer to line vias** where the vias are disclosed to have a width less than 70 nm or an aspect ratio greater than about 4.1 (see Abstract; Figures)

Even assuming *arguendo*, a proper motivation for combination, the combination of Karasawa, Zhou et al., and Chen et al., such combination fails to produce Applicants disclosed and claimed invention.

U.S.S.N. 10,797,945

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

2. Claim 26 stands rejected under 35 USC Section 103(a) as being unpatentable over Karasawa et al. in view of Zhou et al. and Chen et al., above, and further in view of Ono (IEE Trans on Electronic Devices, Vol. 42, No. 10, 1995).

Applicants reiterate the comments made above with respect to Karasawa et al., Zhou et al., and Chen et al.

The further fact that Ono discloses a gate length of less than about 45 nm without a disclosure or teaching of a contact interconnect structure does not further help Examiner in producing Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the

U.S.S.N. 10,797,945

reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

3. Claims 32-35, and 37 stand rejected under 35 USC Section 103(a) as being unpatentable over Karasawa et al. in view Chen et al., above.

Applicants reiterate the comments made above with respect to Karasawa et al. and Chen et al.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Conclusion

The cited references, singly or in combination fail to produce Applicants disclosed and claimed invention, and therefore fail to make out a *prima facie* case of obviousness make out a

U.S.S.N. 10,797,945

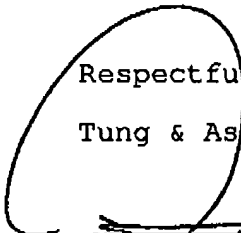
prima facie case of obviousness.

Applicants have amended their claims and have added new claims to clarify Applicants disclosed and claimed invention. Based on the foregoing, Applicants respectfully submit that Applicants Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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